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EXAMINER

SWICKHAMER, CHRISTOPHER M

ART UNIT PAPER NUMBER

2697

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9

Please find below and/or attached an Office communication concerning this application or proceeding.

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# Office Action Summary

Application No.

09/523,572

Applicant(s)

MONIOT, PASCAL

Examiner

Christopher M Swickhamer

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 14 July 2003.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 19 and 20 is/are allowed.
- 6) ☒ Claim(s) 1-4, 7, 9-12 and 14-17 is/are rejected.
- 7) ☒ Claim(s) 5, 6, 8, 13 and 18 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☒ The proposed drawing correction filed on 14 July 2003 is: a) ☒ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

## Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

## Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413) Paper No(s) \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other:

**DETAILED ACTION**

***Response to Amendment***

1. This Office Action is in response to the Amendment filed 07/14/03. Claims 19 and 20 have been added. The amendments to claims 1-18 have been entered. The Examiner approves the changes to the drawings. The 112 2<sup>nd</sup> paragraph rejections to claims 1-6 have been withdrawn due to amendment. Claims 1-20 are pending. Claims 19 and 20 are in condition for allowance. The previous rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Wicklund (USP 6,034,958) to claims 1-18.

***Claim Rejections - 35 USC § 102***

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-4, 7, 9-12 and 14-17 are rejected under 35 U.S.C. 102(e) as being anticipated by Wicklund (USP 6,034,958).

- Referring to claim 1, Wicklund discloses a device for associating channel identifiers (indexes) to ATM PHY/VPI/VCI addresses chosen from among a greater number of values than the number of available channel identifiers (indexes, col. 2, lns. 45-col. 3, lns. 15), including: a search table (memory) containing channel identifiers (indexes) and respective PHY/VPI/VCI combination fields (check words) corresponding to predetermined bits of the ATM

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PHY/VPI/VCI addresses associated with the channel identifiers (indexes, Fig. 4, col. 6, lns. 35-65); a hashing (packing) circuit receiving a current ATM PHY/VPI/VCI address and suppressing in this address bits determined by a generating polynomial pattern such that the suppressed bits correspond to bits of the PHY/VPI/VCI combination fields (check words, Fig. 4, col. 5, lns. 45-67), the hash coded (packed) address provided by the hashing (packing) circuit being used to select in a read mode a search table (memory) location (Fig. 4, col. 5, lns. 57-67); and a comparator configured to indicate that the current ATM PHY/VPI/VCI address corresponds to the selected search table (memory) location when the bits of the PHY/VPI/VCI combination field (check word) of the selected search table location are equal to the corresponding bits of the current ATM PHY/VPI/VCI address (Fig. 4, col. 7, lns. 3-27).

- Referring to claim 2, Wicklund discloses the device of claim 1, wherein the device includes a VCI mask circuit that, according a predetermined VCI mask, annuls bits other than those suppressed by the hashing (packing) circuit, which also correspond to PHY/VPI/VCI combination (check word) bits (col. 4, lns. 50-col. 5, lns. 40).

- Referring to claim 3, Wicklund discloses the device of claim 1, wherein each search table (memory) location contains a High and Low enable bits indicating whether the location is occupied by the correct PHY/VPI/VCI combination field or not.

- Referring to claim 4, Wicklund discloses the device of claim 1, wherein the addresses are ATM network addresses, and the indexes identify connections of the device to one or several ATM networks (col. 2, lns. 45-col. 3, lns. 15).

- Referring to claim 7, Wicklund discloses an address association device, comprising: a VCI masking circuit configured to receive a plurality of ATM address bits and mask the VCI

address bits in accordance with a predetermined VCI mask pattern (col. 4, lns. 50-col. 5, lns. 40); a hashing (packing) circuit configured to receive ATM PHY/VPI/VCI address bits from the masking circuit and to reduce the number of ATM PHY/VPI/VCI address bits to a plurality of hash code (index) bits and to suppress a plurality of PHY/VPI/VCI combination (check word) bits from the ATM address according to a predetermined generating polynomial hashing (packing) pattern (col. 5, lns. 40-67); a search table (memory) configured to receive the plurality of pointer bits found from the hash code bits (index bits) and the plurality of PHY/VPI/VCI combination (check word) bits and to associate the received pointer (index) bits and PHY/VPI/VCI combination (check word) bits with the search table (memory) location of a network connection identified by the channel identifier (Fig. 4, col. 5, lns. 57-col. 6, lns. 12, col. 6, lns. 35-col. 7, lns. 3); and a comparator coupled to the search table (memory) and configured to receive the plurality of ATM PHY/VPI/VCI address bits and to indicate when selected bits from the plurality of ATM PHY/VPI address bits correspond to the plurality of PHY/VPI/VCI combination field (check word) bits associated with the search table (memory) location addressed in the plurality of address bits (col. 7, lns. 3-27).

- Referring to claim 9, Wicklund discloses the device of claim 7 wherein each network connection in the search table (memory) includes a High and Low enable bits that are configured to signal when the network connection in memory is a non-errored active connection to the network (Fig. 4, col. 7, lns. 2-27).

- Referring to claim 10, Wicklund discloses the device of claim 9, further comprising a search logic circuit coupled to the High and Low enable bits and to the comparator and

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configured to indicate when a selected search table location addressed by the plurality of address bits is a non-errored active location (Fig. 4, col. 7, lns. 2-27).

- Referring to claim 11, Wicklund discloses the circuit of claim 7, further comprising a Pointer lookup table (register) configured to store a root (base) address corresponding to a beginning address in the search table (memory) and, further comprising an adder for adding the pointer containing the root (base) address to the hash coded address bits received from the hashing (packing) circuit (Fig. 4, col. 5, lns. 57-67).

- Referring to claim 12, Wicklund discloses a method for associating ATM PHY/VPI/VCI addresses to search table (memory) locations, comprising: receiving a plurality of ATM PHY/VPI/VCI address bits and VCI masking the address bits in accordance with a predetermined VCI mask pattern (Fig. 4, col. 4, lns. 50- col. 5, lns. 40); hashing (packing) the masked plurality of address bits to reduce the number of address bits to a plurality of hash coded (packed) address bits according to a predetermined generating polynomial (packing) pattern and suppressing PHY/VPI/VCI combination (check word) bits from the VCI masked address bits (col. 5, lns. 40-67); associating the hash coded (packed) bits with a pointer to a search table (memory) location corresponding to a network connection identified by the channel identifier (Fig. 4, col. 5, lns. 57-67, col. 7, lns. 2-27); and comparing selected bits from the plurality of ATM PHY/VPI/VCI address bits for a selected search table (memory) location with selected PHY/VPI/VCI combination field bits associated with a search table (memory) location addressed in the plurality of address bits and indicating when there is a match (Fig. col. 7, lns. 2-27).

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- Referring to claim 14, Wicklund discloses the method of claim 12, further comprising logically combining (ANDing) an enable bit with the results of the comparing to determine if a selected memory location is a non-errored active connection.

- Referring to claim 15, Wicklund discloses the method of claim 12 wherein hashing (packing) comprises storing a base pointer lookup table address corresponding to a pointer to a root (beginning) address in a search table (memory) and the method further comprises adding the base pointer lookup table address to the hash coded (packed) address bits reduced during hashing (packing) to determine the root search table address (Fig. 4, col. 5, lns. 40-67, col. 6, lns. 65-col. 7, lns. 27).

- Referring to claim 16, Wicklund discloses the method of claim 12 wherein hashing (packing) further comprises reducing the plurality of ATM PHY/VPI/VCI address bits to the hash coded (packed) address bits by suppressing bits according to a predetermined generating polynomial pattern (col. 5, lns. 40-67).

- Referring to claim 17, Wicklund discloses the method of claim 14, further comprising disabling an enable bit corresponding to a memory location selected by the plurality of address bits when the memory location is occupied. The search table inherently contains a bit indicating whether the location is occupied or not that can be disabled or enabled based on the occupation status of the location. The system must have some way of identifying which locations contain the PHY/VPI/VCI combination fields.

***Allowable Subject Matter***

4. Claims 5, 6, 8, 13 and 18 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

- Claims 19 and 20 are allowable for reasons indicated in the previous Office Action, paper No. 7.

***Response to Arguments***

5. Applicant's arguments with respect to claims 1-18 have been considered but are moot in view of the new ground(s) of rejection.

***Conclusion***

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

- Goubert et al, USP 5,481,687. *Method for reducing the number of bits in a binary word representing a series of addresses.*
- Calamvokis, USP 5,555,256. *Channel Identifier Generation.*
- Bitz et al, USP 5,479,401. *ATM cell interface and method for dispatching an ATM cell.*

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christopher M Swickhamer whose telephone number is (703) 306.4820. The examiner can normally be reached on 8:00-4:30 M-F.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hassan Kizou can be reached on (703) 305-4744. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305.3900.

CMS  
September 16, 2003



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